EE105 Microelectronic Devices and Circuits Frequency Response

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High Frequency Response





Capacitors in MOS Device



$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

$$C_{gd} = C_{ov}$$

$$C_{sb} = C_{jsb} (area + perimeter) junction$$

$$C_{db} = C_{jdb} (area + perimeter) junction$$





(Simplified) High-Frequency Equivalent-Circuit Model for MOSFET



Capacitances between source/body, C_{sb} , and between drain/body, C_{db} , are neglected





Intrinsic Response of FET: Unity-Gain Frequency, f_T

 f_T : defined as frequency at which short-circuit current gain = 1

 f_T : a figure-of-merit for transistor speed



Drain is grounded (short-circuit load)

As gate length reduces in advanced technology node, C_{gs} reduces and $f_T \leftarrow$ increases







Common-Source Voltage Amplifier



- Small-signal model:
- C_{sb} is connected to ground on both sides, therefore can be ignored
- Can solve problem directly by nodal analysis or using 2-port models of transistor
- OK if circuit is "small" (1-2 nodes)

We can find the complete transfer function of the circuit, but in many cases it's good enough to get an estimate of the -3dB bandwidth





CS Voltage Amp Small-Signal Model



For now we will ignore C_{db} to simplify the math





Frequency Response

KCL at input and output nodes; analysis is made complicated

$$\frac{V_{out}}{V_{in}} = \frac{-g_m [r_o \parallel R_L] (1 - j\omega / \omega_z)}{(1 + j\omega / \omega_{p1}) (1 + j\omega / \omega_{p2})}$$

Low-frequency gain:

Two Poles

$$\frac{V_{out}}{V_{in}} = \frac{-g_m \left[r_o \parallel R_L\right] \left(1 - j0\right)}{\left(1 + j0\right) \left(1 + j0\right)} \rightarrow -g_m \left[r_o \parallel R_L\right]$$

Zero:







Calculating the Poles

$$\omega_{p1} \approx \frac{1}{R_s \left\{ C_{gs} + \left(1 + g_m R'_{out}\right) C_{gd} \right\} + R'_{out} C_{gd}}$$

$$\omega_{p2} \approx \frac{R'_{out} / R_s}{R_s \left\{ C_{gs} + \left(1 + g_m R'_{out}\right) C_{gd} \right\} + R'_{out} C_{gd}}$$

Results of complete analysis: not exact and little insight

These poles are calculated after doing some algebraic manipulations on the circuit. It's hard to get any intuition from the above expressions. There must be an easier way!





Method: The Miller Effect



Derive input impedance (assume gain of amplifier = A):





The Miller Effect



Derive input impedance (assume gain of amplifier = A):

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{V_{in}}{(V_{in} - V_{out})/Z_f} = \frac{V_{in}Z_f}{V_{in} - AV_{in}} = \frac{Z_f}{1 - A}$$

Consider the case where Z_f is a capacitor

$$Z_f = \frac{1}{sC} \Rightarrow Z_{in} = \frac{1}{s(1-A)C}$$

- For negative A, input impedance sees increased cap value
- For A = 1, input impedance sees no influence from cap
- For A > 1, input impedance sees negative capacitance!





Using The Miller Effect



Notice that C_{gd} is in the feedback path of the common source amplifier

– Recall Miller effect calculation: $C_{in} = (1 - A)C_{gd}$

Effective input capacitance:

$$C_{in} = \frac{1}{j\omega C_{Miller}} = \left(\frac{1}{1 - A_{v,Cgd}}\right) \left(\frac{1}{j\omega C_{gd}}\right) = \frac{1}{j\omega \left[\left(1 - A_{vCgd}\right)C_{gd}\right]}$$



CS Voltage Amp Small-Signal Model

Modified Small-Signal Model with Miller Effect:



- We can approximate the first pole by using Miller capacitance
- This gives us a good approximation of the -3dB bandwidth





Comparison with "Exact Analysis"

Miller result (calculate RC time constant of input pole):

$$\omega_{p1}^{-1} = R_{S} \left[C_{gs} + \left(1 + g_{m} R_{out}' \right) C_{gd} \right]$$

Exact result:

$$\omega_{p1}^{-1} = R_{S} \left[C_{gs} + (1 + g_{m} R_{out}') C_{gd} \right] + R_{out}' C_{gd}$$

As a result of the Miller effect there is a fundamental gain-bandwidth tradeoff





Common Drain Amplifier



Calculate Bandwidth of the Common Drain (Source-Follower)

Procedure:

- 1. Replace current source with MOSFET-based current mirror
- 2. Draw small-signal model with capacitors (for simplicity, we will focus on C_{gd} and C_{gs})
- 3. Find the DC small-signal gain
- 4. Use the Miller effect to calculate the input capacitance
- 5. Calculate the dominant pole





Two-Port CD Model with Capacitors



- Find DC Gain
- Find Miller capacitor for C_{gs} -- note that the gatesource capacitor is between the input and output!





Voltage Gain Across C_{gs}

Write KCL at output node:







Compute Miller Effected Capacitance

Now use the Miller Effect to compute C_{in} : Remember that C_{gs} is the capacitor from the input to the output







Bandwidth of Source Follower

Input low-pass filter's –3 dB frequency:

$$\omega_{p}^{-1} = R_{S} \left(C_{gd} + \frac{C_{gs}}{1 + g_{m}(r_{o} \| r_{oc})} \right)$$

Substitute favorable values of R_s , r_o :

$$\begin{split} R_{S} \approx 1/g_{m} & r_{o} \gg 1/g_{m} \\ \omega_{p}^{-1} \approx (1/g_{m}) \left(C_{gd} + \frac{C_{gs}}{1 + BIG} \right) \approx C_{gd} / g_{m} \\ \omega_{p} \approx g_{m} / C_{gd} & \end{split}$$
 Very high frequency! Model not valid at these high frequencies



Some Examples

Common Source Amplifier:

 A_{vCgd} = Negative, large number (-100)

$$C_{Miller} = (1 - A_{V,C_{gd}}) C_{gd} \approx 100 C_{gd}$$

Miller Multiplied Cap has <u>detrimental</u> impact on bandwidth

<u>Common Drain Amplifier:</u>

 A_{vCgs} = Slightly less than 1

$$C_{Miller} = (1 - A_{V,Cgs})C_{gs} \simeq 0$$

"Bootstrapped" cap has negligible impact on bandwidth!



Open-Circuit Time Constant (OCTC) Method for High Cut-off Frequency

- 1. Replace all capacitance by open circuit
- 2. Replace signal source by short circuit
- 3. Consider one capacitor at a time, find resistance *R_i* "seen" by the i-th capacitor, *C_i*4.

$$\omega_{H} \approx \frac{1}{\sum_{i} C_{i} R_{i}}$$







Applying OCTC to CS Amplifier

$$\tau_{H} = R_{sig}^{'}C_{gs} + (R_{sig}^{'}(1 + g_{m}R_{L}^{'}) + R_{L}^{'})C_{gd} + R_{L}^{'}C_{L}$$

Rearranging :

$$\tau_{H} = R_{sig}^{'}C_{gs} + \left(R_{sig}^{'}(1+g_{m}R_{L}^{'})+R_{L}^{'}\right)C_{gd}$$

= $R_{sig}^{'}C_{gs} + R_{sig}^{'}(1+g_{m}R_{L}^{'})C_{gd} + R_{L}^{'}C_{gd} + R_{L}^{'}C_{L}$
 $\approx R_{sig}^{'}\left(C_{gs} + (1+g_{m}R_{L}^{'})C_{gd}\right) + R_{L}^{'}\left(C_{gd} + C_{L}\right)$

Time constant from input port of Miller Equivalent Circuit Time constant from Output port of Miller Equivalent Circuit





High-Frequency Response of CG Amplifier

Note: C_{gd} and C_L can be lumped togetheer

since they are in parallel.



- No Miller effect since both capacitance are grounded
- The dominant term is likely to be $(1/g_m)C_{gs}$, which is small \rightarrow High f_H
- → Common-Gate is a broadband amplifier

